IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please enter the title as amended.

~~FLIP CHIP~~ FLIP-CHIP ADAPTOR PACKAGE FOR BARE DIE

IN THE SPECIFICATION:

Please amend the first full paragraph on page 2, together with the section title immediately preceding it as follows:

~~CROSS REFERENCE~~ CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of application Serial No. 09/483,483, filed January 14, 2000, ~~pending,~~ now U.S. Patent 6,265,766 B1, issued July 24, 2001, which is a continuation of application Serial No. 08/948,936, filed October 10, 1997, now U.S. Patent 6,201,304 B1, issued March 13, 2001, which is a continuation of application Serial No. 08/574,662, filed December 19, 1995, now U.S. Patent 5,719,440, issued February 17, 1998.

Please amend the fifth full paragraph on page 2 as follows:

COB - Chip On Board: The techniques used to attach semiconductor dice to a printed circuit board, including ~~flip chip~~ flip-chip attachment, ~~wirebonding,~~ wire bonding, and tape automated bonding ("TAB").

Please amend the first full paragraph on page 3 as follows:

~~Flip Chip:~~ Flip-Chip: A chip or die that has bumped terminations spaced around the active surface of the die and is intended for facedown mounting.

Please amend the second full paragraph on page 3 as follows:

~~Flip Chip~~ Flip-Chip Attachment: A method of attaching a semiconductor die to a substrate in which the die is flipped so that the connecting conductor pads on the face of the die are set on mirror-image pads on the substrate (i.e. printed circuit board) and bonded by refluxing the solder.

Please amend the sixth full paragraph on page 3 as follows:

State-of-the-art COB technology generally consists of three semiconductor dies to printed circuit boards attachment techniques: ~~flip chip~~ flip-chip attachment, ~~wirebonding,~~ wire bonding, and TAB.

Please amend the paragraph bridging pages 3 and 4 as follows:

~~Flip chip~~ Flip-chip attachment consists of attaching a semiconductor die, generally having a BGA, a SLICC or a PGA, to a printed circuit board. With the BGA or SLICC, the solder ball arrangement on the semiconductor die must be a mirror-image of the connecting bond pads on the printed circuit board such that precise connection is made. The semiconductor die is bonded to the printed circuit board by refluxing the solder balls. With the PGA, the pin arrangement of the semiconductor die must be a mirror-image of the pin recesses on the printed circuit board. After insertion, the semiconductor die is generally bonded by soldering the pins into place. An under-fill encapsulant is generally disposed between the semiconductor die and the printed circuit board to prevent contamination. A variation of the pin-in-recess PGA is a J-lead PGA, wherein the loops of ~~the J's~~ the Js are soldered to pads on the surface of the circuit board. Nonetheless, the lead and pad locations must coincide, as with the other referenced flip-chip techniques.

Please amend the first full paragraph on page 4 as follows:

~~Wirebonding~~ Wire bonding and TAB attachment generally begins with attaching a semiconductor die to the surface of a printed circuit board with an appropriate adhesive. In ~~wirebonding,~~ wire bonding, a plurality of bond wires are attached, one at a time, from each bond pad on the semiconductor die and to a corresponding lead on the printed circuit board. The bond wires are generally attached through one of three industry-standard ~~wirebonding~~ wire bonding techniques: ultrasonic ~~bonding~~ bonding, using a combination of pressure and ultrasonic vibration bursts to form a metallurgical cold weld; thermocompression ~~bonding~~ bonding, using a combination of pressure and elevated temperature to form a weld; and thermosonic ~~bonding using~~ bonding, using a combination of pressure, elevated temperature, and ultrasonic vibration

bursts. The die may be oriented either face up or face down (with its active surface and bond pads either up or down with respect to the circuit board) for wire bonding, although face up orientation is more common. With TAB, metal tape leads are attached between the bond pads on the semiconductor die and the leads on the printed circuit board. An encapsulant is generally used to cover the bond wires and metal tape leads to prevent contamination.

Please amend the second full paragraph on page 4 as follows:

Although the foregoing methods are effective for bonding semiconductor ~~dies~~ dice to printed circuit boards, the terminal arrangements of the ~~dies~~ dice and the connection arrangements of the boards must be designed to accommodate one another. Thus, it may be impossible to electrically connect a particular semiconductor die to a printed circuit board for which the semiconductor die terminal arrangement was not designed to match the board's connection arrangement. With either ~~wirebond~~ wire bond or TAB attachment, the semiconductor die bond pad may not correspond to the lead ends on the circuit board, and thus attachment is either impossible or extremely difficult due to the need for overlong wires and the potential for inter-wire contact and shorting. With ~~flip chip~~ flip-chip attachment, if the printed circuit board connection arrangement is not a mirror-image of the solder ball or pin arrangement (terminal arrangement) on the semiconductor die, electrically connecting the ~~flip chip~~ flip-chip to the printed circuit board is impossible.

Please amend the second full paragraph on page 5 as follows:

The present invention relates to an intermediate printed circuit board or other conductor-carrying substrate that functions as an adaptor board for electrically connecting one or more bare semiconductor ~~dies~~ dice of a variety of sizes and bond pad locations, solder ball arrangement, or pin arrangement, to a master printed circuit board with a specific or standardized pin out, connector pad location, or lead placement.

Please amend the paragraph bridging pages 5 and 6 as follows:

On the semiconductor die side of the adaptor board, one or more semiconductor ~~dies~~ dice are attached. If a ~~"flip-chip"~~ "flip-chip" die is attached to the adaptor board, the adaptor board will, of course, be configured with an I/O pattern to receive the ~~flip chip~~ flip-chip with a specific pin out or connector pad locations. The pin out or connector pads on the adaptor board are connected to circuit traces on or through the adaptor board. The circuit traces form the electrical communication path from the pin recesses or connector pads on the adaptor board to the connection points to the master board.

Please amend the first full paragraph on page 6 as follows:

If a "leads over" die is used with the adaptor board, the bond pads on the die are ~~wirebonded~~ wire bonded to the adaptor board. Preferably, the leads over die is attached to the adaptor board with the bond pads facing the adaptor board. The bond wires are attached to the leads over die bond pads and extend into a via or vias in the adaptor board. The bond wires are attached to an I/O pattern of adaptor board bond pads within the via from which circuit traces extend, or to leads on the master board side of the adaptor board.

Please amend the third full paragraph on page 6 as follows:

Preferably, the exposed circuitry of the die and the die-to-adaptor board interconnection is sealed from contamination by a glob top after wire bonding or an underflow compound in the case of a ~~flip chip attach.~~ flip-chip attachment.

Please amend the second full paragraph on page 7 as follows:

FIG. 1 illustrates a first embodiment of the present invention designated as a ~~flip chip style/flip chip attach~~ flip-chip style/ flip-chip attachment assembly 100. Assembly 100 comprises a semiconductor die 12 having an inverted active surface 14 with at least one ~~flip chip~~ flip-chip electric connection 16 (such as a C4 solder bump connection, a pin connection, or a surface mount j-lead connection, by way of example) extending substantially perpendicularly

from a bond pad 15 on the semiconductor die active surface 14. The ~~flip chip~~ flip-chip electric connections 16 are attached to an upper surface 20 of an adaptor board 18 in such a manner that the ~~flip chip~~ flip-chip electric connections 16 make electrical contact with electrical contact elements 21 in or on the surface of adaptor board 18. The electrical contact elements 21 make electrical communication between each ~~flip chip~~ flip-chip electric connection 16, through circuit traces 23 (exemplary traces shown in broken lines) in the adaptor board 18, to at least one master board connector 22 extending substantially perpendicularly from a lower surface 24 of the adaptor board 18 to connect adaptor board 18 to an aligned terminal 31 on master board 30. Preferably, a sealing compound 26 is disposed between the semiconductor die 12 and the adaptor board 18 to prevent contamination of the ~~die-to-adaptor board~~ flip-chip electric connections 16 and to more firmly secure semiconductor die 12 to adaptor board 18.

Please amend the paragraph bridging pages 7 and 8 as follows:

FIGS. 2 and 2A illustrate a second embodiment of the present invention designated as a ~~flip chip~~ flip-chip style/wire bond ~~attach~~ attachment assembly 200. Components common to both FIG. 1 and FIG. 2 retain the same numeric designation. The assembly 200 comprises the semiconductor die 12 having ~~lower~~ active surface 14 with at least one ~~flip chip~~ flip-chip electric connection 16, as known in the art, extending substantially perpendicularly from a bond pad 15 on the semiconductor die ~~lower~~ active surface 14. The ~~flip chip~~ flip-chip electric connections 16 are attached to the adaptor board upper surface 20 in such a manner that the ~~flip chip~~ flip-chip electric connections 16 make electrical contact with electrical contact elements 21 on the adaptor board 18. The electrical contact elements 21 communicate between each ~~flip chip~~ flip-chip electric connection 16 to bond pads 28 on the adaptor board upper surface 20 through circuit traces 23. The adaptor board lower surface 24 is bonded to an upper surface 36 of a master board 30 with an adhesive 32, which may comprise a liquid or gel adhesive, or an adhesive tape, all as known in the art. If desired, adhesive 32 may be a heat-conductive adhesive. A wire bond 34 extends from each adaptor board bond pad 28 to a corresponding bond pad or lead end 35 on the upper surface 36 of master board 30, bond pad or lead end 35 communicating

with other components mounted to master board 30 or with other components on other boards or other assemblies through circuit traces or other conductors known in the art.

Please amend the paragraph bridging pages 8 and 9 as follows:

FIGs. 3 and 3A illustrate a third embodiment of the present invention designated as a wire bond ~~style/flip-chip attach~~ style/flip-chip attachment assembly 300. Components which are common to the previous figures retain the same numeric designation. The assembly 300 comprises an inverted semiconductor die 12 having ~~lower~~ active surface 14 with at least one bond pad 38 on the semiconductor die ~~lower~~ active surface 14. As illustrated, the bond pads 38 are arranged in two rows extending down the longitudinal axis of semiconductor die 12 being located transverse to the plane of the page, such an arrangement commonly being used for a "leads over" connection to frame leads extending over the die in its normal, upright position. The semiconductor die ~~lower~~ active surface 14 is bonded to the adaptor board upper surface 20 with an insulating, sealing adhesive 40. The adaptor board 18 includes at least one or more wire bond ~~via~~ vias 42 which is located in a position or positions aligned with the semiconductor die bond pads 38. Each individual wire bond 134 is connected to each corresponding individual semiconductor die bond pad 38. Each wire bond 134 extends from the semiconductor die bond pad 38 to a corresponding bond pad or lead 39 on the adaptor board lower surface 24, which communicates with ~~adaptor~~ master board connectors 22 through circuit traces 23. The master board terminals 31 are in electrical communication with at least one ~~adaptor~~ master board connector 22 extending substantially perpendicularly from the ~~adapter~~ adaptor board lower surface 24. Preferably, a sealant 44 encases the bond wires 134 and seals the wire bond via 42 to prevent contamination and damage to the wire bonds.

Please amend the first full paragraph on page 9 as follows:

FIG. 4 illustrates a fourth embodiment of the present invention designated as a wire bond style/wire bond ~~attach~~ attachment assembly 400. Components which are common to the previous figures retain the same numeric designation. The assembly 400 comprises the

semiconductor die 12 having ~~lower~~ active surface 14 with at least one bond pad 38 on the semiconductor die ~~lower~~ active surface 14. As with the embodiment of FIG. 3, semiconductor die 12 in this instance employs bond pads 38 in a "leads over" configuration. The semiconductor die ~~lower~~ active surface 14 is bonded to the adaptor board upper surface 20 with an insulating, sealing adhesive 40. The adaptor board 18 includes at least one wire bond via 42 which is located in a position or positions aligned with the semiconductor die bond pads 38. Each individual wire bond 134 is connected to each corresponding semiconductor die bond pad 38. Each wire bond 134 extends from the semiconductor die bond pad 38 to a corresponding bond pad 46 within the wire bond via 42. The via bond pads 46 are in electrical communication through circuit traces 23 with at least one corresponding ~~adapter~~ adaptor board bond pad 28. The adaptor board lower surface 24 is bonded to the master board upper surface 36 with the adhesive 32. Wire bonds 34 extend from the adapter board upper surface 20 to a corresponding bond pad or lead on the master board upper surface 36. Preferably, the wire bond via sealant 44 encases the bond wires 134 and seals the wire bond via 42 to prevent contamination.